Friedrich-Alexander-Universität
Naturwissenschaftliche Fakultät

Department of
DATA SCIENCE

Fraunhofer
IIS

Master's thesis:

Place and Route Optimization for Chip Design

Topic description

The design of integrated circuits involves challenging tasks such as the placement of circuit elements and the routing of interconnections. Seeking an optimal or at least feasible design leads to optimization problems with an objective that include, e.g., power consumption, delays and performance criteria.

We aim to investigate these problems in the context of spiking neural networks, executed on neuromorphic hardware. A preliminary step would be to analyze the special requirements for this kind of hardware and implications for the usability of existing methods (e.g., [1–5]). Then we want to explore optimization methods for the placement and routing problems. In particular, the following aspects would be of interest: deciding on the feasibility of the routing problem very fast, identifiying re-placement options in cases of routing infeasibility, and integrating the two problems into one two-stage problem.

Prior knowledge of mixed-integer and combinatorial optimization as well as basic programming skills (python) are required.

This thesis will be supervised jointly by the the Department of Data Science (Frauke Liers) and the Fraunhofer IIS.

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In case of interest please send an email including a Transcript of Records, a short Letter of Motivation as well as a preferred starting date.

References

[1] Michael Gester, Dirk Müller, Tim Nieberg, Christian Panten, Christian Schulte, and Jens Vygen. BonnRoute: Algorithms and data structures for fast and good VLSI routing. *ACM Transactions on Design Automation of Electronic Systems*, 18(2):1–24, March 2013. ISSN 1084-4309, 1557-7309. doi: 10.1145/2442087.2442103. URL https://dl.acm.org/doi/10.1145/2442087.2442103.

[2] Yuanfang Hu. *On-chip interconnection architecture optimization using a multicommodity flow approach*. PhD thesis, UC San Diego, 2007.

[3] Bernhard Korte, Dieter Rautenbach, and Jens Vygen. BonnTools: Mathematical Innovation for Layout and Timing Closure of Systems on a Chip. *Proceedings of the IEEE*, 95(3):555–572, 2007. ISSN 0018-9219. doi: 10.1109/JPROC.2006.889373. URL http://ieeexplore.ieee.org/document/4167775/.

[4] L. McMurchie and C. Ebeling. PathFinder: A Negotiation-Based Performance-Driven Router for FPGAs. In *Third International ACM Symposium on Field-Programmable Gate Arrays*, pages 111–117, Napa Valley, CA, USA, 1995. IEEE. ISBN 978-0-7695-2550-1. doi: 10.1109/FPGA.1995.242049. URL http://ieeexplore.ieee.org/document/1377269/.

[5] Yue Zha and Jing Li. Revisiting PathFinder Routing Algorithm. In *Proceedings of the 2022 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, pages 24–34, Virtual Event USA, February 2022. ACM. ISBN 978-1-4503-9149-8. doi: 10.1145/3490422.3502356. URL https://dl.acm.org/doi/10.1145/3490422.3502356.