Friedrich-Alexander-Universität
Naturwissenschaftliche Fakultät

Department of
DATA SCIENCE

Fraunhofer
IIS

**Master's thesis:**

# Automated testing of circuit-switched Networks-on-Chip for chip design

## Topic description

The design of integrated circuits involves challenging tasks such as testing manufactured hardware for defects. This especially applies to circuit-switched networks-on-chip (NoCs) as they allow a variety of physical connections from one source node to one or many sink nodes on the hardware via software configuration. Malfunctioning connections shall be identified such that they can be bypassed later.

Consequently, an optimized automated testing strategy is required that can guarantee the correct working of the NoC and, at least roughly, localizes errors in the silicon in the shortest time possible. We aim to investigate this in the context of a circuit-switched NoC implementation of a spiking neural network hardware accelerator. A preliminary step would be to mathematically model the NoC. Then we want to explore strategies that allow the testing to start with as few global connections as needed, which can be decomposed into increasingly local connections to pin down hardware defects to single wires or switch boxes. While a correctness guarantee of the hardware test is of utmost importance, parallel testing of connections is also of great interest as this would heavily decrease the runtime.

Prior knowledge of mixed-integer and combinatorial optimization as well as basic programming skills (python) are required.

This thesis will be supervised jointly by the the Department of Data Science (Frauke Liers) and the Fraunhofer IIS.

## Contact

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*In case of interest please send an email including a Transcript of Records, a short Letter of Motivation as well as a preferred starting date.*